REMARKS

Claims 14-19 are pending in the present application.

In response to the Notice of Non-Compliant Amendment mailed October 25, 2002, clean and marked-up versions of replacement paragraphs have been provided. In addition, minor informalities have been corrected in claims 30-33.

This Amendment is in response to the Office Action mailed May 1, 2002. In the Office Action, the Examiner rejected claims 14-16 under 35 U.S.C. §112; and claims 14, 17 and 18 under 35 U.S.C. §103(a). In addition, the Examiner indicated allowable subject matter for claims 15, 16 and 19 if they are rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants have amended claims 14-19, and added claims 20-33. Applicants submit that the newly-added claims introduce no new matter. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

I. SPECIFICATION

The Examiner objected to the Specification due to minor informalities. Specifically, the Examiner stated that the description of the related art is missing. In response, Applicants have amended the Specification to change the heading "BACKGROUND OF THE INVENTION" to "DESCRIPTION OF THE RELATED ART". Therefore, Applicants respectfully request the objection be withdrawn.

II. REJECTION UNDER 35 U.S.C. §112

In the Office Action, the Examiner rejected claims 14-16 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Applicants have amended claims 14-16 to clarify the claim language. Therefore, Applicants respectfully request the rejection under 35 U.S.C. §112 be withdrawn.

III. REJECTION UNDER 35 U.S.C. §103(A)

In the Office Action, the Examiner rejected claim 14 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,013,681 issued to Godbey et al. ("Godbey") in view of U.S. Patent No. 5,310,451 issued to Tejewani et al. ("Tejewani"). The Examiner also rejected claims 17 and 18 as being unpatentable over Tejewani in view of Godbey. Applicants respectfully traverse the rejections for the following reasons.

Godbey discloses a method of producing a thin silicon-on-insulator (SOI) layer. Silicon Germanium alloy is used as an etch stop in bond-and-etchback SOI technology (Godbey, col. 6, lines 10-16).

Tejewani discloses a method of forming an ultra-uniform silicon-on-insulator layer. A first strain-free etch stop layer is formed on top surface of primary substrate (Tejewani, col. 5, lines 47-49). On top of the first strain-free etch stop layer is one intermediate layer pair comprising a spacer layer and a second strain-free etch stop layer (Tejewani, col. 6, lines 40-68).

Contrary to the Examiner's contention that Tejewani teaches "a strained silicon layer 22 in contact with the relaxed SiGe" (Office Action, page 3, paragraph 6, last line), the intermediate layer pair 22 comprises only a spacer layer and a strain-free layer. Therefore, in effect, Tejewani teaches away use of strained silicon layer.

There is no motivation to combine Godbey and Tejewani because neither of them addresses the problem of transferring a strained silicon layer to a silicon oxide layer. There is no teaching or suggestion that a strained silicon layer on top of a silicon oxide is present. Godbey and Tejewani, read as a whole, does not suggest the desirability of transferring a strained silicon layer to a silicon oxide layer. For the above reasons, the rejection under 35 U.S.C. §103(a) is improperly made.

Godbey and Tejewani, taken alone or in any combination, do not disclose, suggest, or render obvious transferring a strained silicon layer to a silicon oxide layer.

To clarify the claim language, claims 14-19 have been amended. In addition, new claims 20-33 are added without introducing new matter.

The Examiner failed to establish a prima facie case of obviousness and failed to show there is teaching, suggestion or motivation to combine the references. "When determining the patentability of a claimed invention which combined two known elements, 'the question is whether there is something in the prior art as a whole suggest the desirability, and thus the

obviousness, of making the combination.'" In re Beattie, Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 1462, 221 U.S.P.Q. (BNA) 481, 488 (Fed. Cir. 1984). To defeat patentability based on obviousness, the suggestion to make the new product having the claimed characteristics must come from the prior art, not from the hindsight knowledge of the invention. Interconnect Planning Corp. v. Feil, 744 F.2d 1132, 1143, 227 U.S.P.Q. (BNA) 543, 551 (Fed. Cir. 1985). To prevent the use of hindsight based on the invention to defeat patentability of the invention, this court requires the Examiner to show a motivation to combine the references that create the case of obviousness. In other words, the Examiner must show reasons that a skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the prior elements from the cited prior references for combination in the manner claimed. In re ROUFFET, 149 F.3d 1350 (Fed. Cir. 1996), 47 U.S.P.Q.2d (BNA) 1453. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or implicitly suggest the claimed invention or the Examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." Ex parte Clapp, 227 USPQ 972, 973. (Bd.Pat.App.&Inter. 1985).

Therefore, Applicants believe that independent claims 1, 14 and 17 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicants respectfully request the rejections under 35 U.S.C. §112 and 35 U.S.C. §103(a) be withdrawn.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

1. The heading on page 1, line 6, "BACKGROUND OF THE INVENTION" has been replaced as follows:

-- DESCRIPTION OF THE RELATED ART –

2. The paragraph on page 3, line 11; has been amended as follows:

-- The relaxed SiGe layer 102 is formed upon or deposited on top the silicon substrate 101. The strained silicon layer 104 is then formed on the relaxed SiGe layer 102. In one embodiment, the relaxed SiGe layer 102, and the strained silicon layer 104 are formed by an epitaxial growth process. In other words, the process includes epitaxial growth of relaxed SiGe on the silicon wafer 101 to create the relaxed SiGe layer 102, epitaxial growth of a thin silicon film on the stack structure of the silicon wafer 101 to create the strained silicon film 104. The relaxed SiGe layer has the thickness in the range of approximately from 0.1μm to 3.0μm. It is contemplated that the forming of these layers in the stack structure may be done in any other process other than the epitaxial growth process.

3. The paragraph on page 4, line 27; has been amended as follows:

-- Figure 6 is a diagram illustrating Figure 5 with further heat treatment to transfer the strained layer to the oxidized wafer according to one embodiment of the invention. After the lower heat treatment to result the bonding of silicon wafer 101 and oxidized wafer 401, higher temperature heat treatment is applied. This temperature used in this further heat treatment ranges from approximately 400 °C to 600 ° C. The higher temperature heat treatment results in the bonding of surface 104 to wafer ~~101~~ 401 at the SiO2 interface 601. The further heat treatment also results in the separation of the two wafers at the embrittled region (described in Figure 2). After the further heat treatment, the two wafers 101 and 401 are delaminated along the embrittled implanted region (i.e., H-implanted SiGe region). This effectively separates the two wafers and the strained silicon film 104 is transferred to the SOI-like wafer 401. In one embodiment, the embrittled region resides on the relaxed SiGe layer 102. When the two wafers 101 and

401 separate, the strained silicon layer 104 and the part of the relaxed SiGe layer 102 are transferred to the SOI wafer 401. Part of relaxed SiGe layer 102 is then etched off to result the wafer 401 with the strained silicon layer 104 on top of the SiO_2 layer. This results in the transfer of the strained silicon layer 104 to the SOI wafer 401(e.g., oxidized wafer 401). It is contemplated that the etching may be wet or plasma etching; however, wet etching is used to better remove the entire SiGe residue on the strained silicon film.

4. The paragraph on page 5, line 14; has been amended as follows:

-- In one embodiment where there is no implanting step (i.e., hydrogen implant), the embrittled region is not formed. The strained silicon layer ~~103~~ 104 is transferred to the SOI wafer 401 by a bonded-etchback process on the silicon wafer 101 and the strained SiGe ~~103~~ 104. This gives the strained silicon film on the SOI wafer 401.--

IN THE CLAIMS

The following is a set of claims showing all amended and new claims.

14. (AMENDED) A ~~wafer~~ device comprising:

a silicon layer;

a relaxed ~~SiGe~~ layer; and

a strained silicon layer in contact with the relaxed ~~SiGe~~ layer, the strained silicon layer ~~being~~ to be transferred to ~~the~~ top of ~~the relaxed SiGe layer~~ a wafer by a heat treatment, the wafer having a base substrate and an oxidized film.

15. (AMENDED) The ~~wafer~~ device of claim 14 ~~wherein the relaxed SiGe layer contains~~ further comprising an embrittled region.

16. (AMENDED) The ~~wafer~~ device of claim 15 wherein the embrittled ~~report~~ region is created by ~~implanting hydrogen ions~~ an ion implantation.

17. (AMENDED) A ~~wafer~~ device comprising:

a silicon layer;

a SiO_2 layer in contact with the silicon layer; and

a strained silicon layer on top of the SiO_2 layer, the strained silicon layer being transferred from a wafer, ~~to an oxidized wafer by a heat treatment~~ the wafer having base substrate and a layer of relaxed film.

18. (AMENDED) The ~~wafer~~ device of claim 17 wherein the ~~oxidized wafer contains~~ relaxed film is a relaxed SiGe layer.

19. (AMENDED) The ~~wafer~~ device of claim 18 wherein the ~~relaxed SiGe layer contains~~ wafer further comprises an embrittled region.

20. (NEW) The device of claim 17 wherein the strained silicon layer is transferred to top of the SiO_2 layer by a bonded-etch back process.

21. (NEW) The device of claim 17 wherein the base substrate is a silicon layer.

22. (NEW) The device of claim 17 wherein the heat treatment uses a temperature range of approximately 400°C to 600°C.

23. (NEW) The device of claim 14 wherein the relaxed layer is a relaxed SiGe layer.

24. (NEW) The device of claim 23 wherein the relaxed SiGe layer has a thickness ranging from 0.1μm to 3.0μm.

25. (NEW) The device of claim 16 wherein the ion implantation uses an energy range of approximately 1keV to 20keV.

26. (NEW) The device of claim 16 wherein the ion implantation uses a dose range of approximately 1E116/cm^3 to 1E18/cm^3.

27. (NEW) The device of claim 16 wherein the ion implantation uses hydrogen ions.

28. (NEW) A wafer structure comprising:

a first wafer having a first base substrate, a relaxed film layer, and a strained film layer, and

a second wafer having a second base substrate and an oxidized film layer, the second wafer being bonded to the first wafer by a fire heat treatment, the strained film layer being transferred to the second wafer after the second wafer is separated from the first wafer by a second heat treatment.

29. (NEW) The wafer structure of claim 28 wherein one of the first and second base substrates is a silicon layer.

30. (NEW) The wafer structure of claim 28 wherein the relaxed film is a relaxed SiGe layer.

31. (NEW) The wafer structure of claim 28 wherein the strained film layer is a strained silicon layer.

32. (NEW) The wafer structure of claim 28 wherein the first heat treatment uses a temperature range of approximately 100°C to 300°C.

33. (NEW) The wafer structure of claim 28 wherein the second heat treatment uses a temperature range of approximately 400°C to 600°C.

CONCLUSION

In view of the amendments and remarks made above, it is respectfully submitted that the pending claims are in condition for allowance, and such action is respectfully solicited.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on: November 19, 2002.

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